

IN THE CLAIMS:

Claims 1 - 12 (Withdrawn)

- 1     13.    (Currently Amended) An integrated circuit having a device layer of  
2     semiconductor with a device layer thickness of less than 100nm above an  
3     array insulating layer and containing an array of DRAM cells including a  
4     trench capacitor connected by a buried strap to a horizontal pass transistor  
5     formed in said device layer, said pass transistor having an internal contact  
6     adjacent said trench, in which:
- 7     said set of trench capacitors have center electrodes insulated by a capacitor  
8     insulator, said center electrodes having a top surface below a bottom  
9     surface of said device layer;
- 10    said buried strap is formed from strap conductive material extending  
11    vertically in said trenches to a level below said bottom surface of said  
12    device layer and laterally outside said trenches and underneath said  
13    internal contact of said pass transistor, whereby said strap conductive  
14    material makes electrical contact with said bottom surface to form said  
15    buried straps; and

16 top insulating material having a top insulator thickness extending up to a  
17 surface of said device layer in said trenches ~~extending~~ above said strap  
18 conductive material and abutting a vertical surface of said internal contact  
of said pass transistor.

1 14. (Original) An integrated circuit according to claim 13, further  
2 having a conformal layer of conductive material extending along a top  
3 surface of said center electrode and said bottom surface of said device  
4 layer.

15. (Withdrawn)

1 16. (New) An integrated circuit having a device layer of semiconductor  
2 with a device layer thickness of less than 100nm above an array insulating  
3 layer and containing an array of DRAM cells disposed in a first subset of  
4 DRAM cells and a second subset of DRAM cells, including a trench  
5 capacitor formed at an edge of said DRAM cells and connected by a buried  
6 strap to a horizontal pass transistor formed in said device layer and  
7 displaced laterally from said trench capacitor, comprising:

8 said set of trench capacitors extending through said device layer and array  
9 insulating layer and having center electrodes insulated by a capacitor  
10 insulator;

11 said center electrodes being recessed below a bottom surface of said device  
12 layer;

13 a contact area on said bottom surface of said device layer outside said  
14 trenches;

15 strap conductive material disposed in said trenches to a level above said  
16 bottom surface of said device layer, whereby said strap conductive material  
17 makes electrical contact with said bottom surface to form said buried  
18 straps;

19 top insulating material having a top insulator thickness extending up to a  
20 surface of said device layer in said trenches above said strap conductive  
21 material, whereby said top insulator thickness is approximately equal to  
22 said device layer thickness; and

23 a set of isolating trenches extending through said device layer and said  
24 array insulating layer outside said trenches and said cell pass transistors, to

25 a depth of at least said bottom of said buried straps, whereby only that  
26 portion of said buried strap inside said trenches and underneath said  
27 transistors remains and said buried straps are isolated from corresponding  
28 buried straps in adjacent cells by said isolating trenches;

29 a set of horizontal cell pass transistors in said device layer having cell  
30 electrodes, transistor gates disposed above said device layer and connected  
31 to a first subset of interconnect lines and internal electrodes in contact with  
32 said buried straps through said contact area and separated from an adjacent  
33 trench by said isolating trenches.

1 17. (New) An integrated circuit according to claim 16, further  
2 comprising:

3 a first subset of interconnect lines contacting transistor gates in said first  
4 subset of cells and extending over trenches in said second subset of cells,  
5 said first subset of interconnect lines passing over and being separated  
6 vertically from said buried straps in said second subset of cells by said top  
7 insulator thickness; and

8 a second subset of interconnect lines contacting transistor gates in said  
9 second subset of cells and extending over trenches in said first subset of

10 cells, said second subset of interconnect lines being separated vertically  
11 from said buried straps in said first subset of cells by said top insulator  
12 thickness.

1 18. (New) An integrated circuit according to claim 16, in which said  
2 strap conductive material in said trenches is disposed only below said  
3 bottom surface of said device layer, whereby said strap conductive material  
4 makes contact with said device layer only on said bottom surface and said  
5 top insulating material has a top insulator thickness greater than said  
6 device layer thickness.

1 19. (New) An integrated circuit having a device layer of semiconductor  
2 with a device layer thickness of less than 100nm above an array insulating  
3 layer and containing an array of DRAM cells disposed in a first subset of  
4 DRAM cells and a second subset of DRAM cells, including a trench  
5 capacitor formed at an edge of said DRAM cells and connected by a buried  
6 strap to a horizontal pass transistor formed in said device layer and  
7 displaced laterally from said trench capacitor, said array of DRAM cells  
8 having at least some pairs of cells having a trench capacitor in a first cell  
9 separated by a portion of material from a corresponding trench capacitor in  
10 an adjacent cell, comprising:

11 said set of trench capacitors extending trenches through said device layer  
12 and array insulating layer and having center electrodes extending below a  
13 bottom surface of said device layer and insulated by a capacitor insulator;  
  
14 a conformal liner of conductive material disposed in said trenches to a  
15 level above said bottom surface of said device layer, whereby said liner of  
16 conductive material makes electrical contact with a bottom surface of said  
17 device layer at the location where said buried strap meets said buried  
18 surface;  
  
19 strap conductive material disposed in said trenches to a level above said  
20 bottom surface of said device layer, whereby said strap conductive material  
21 makes electrical contact with said bottom surface to form said buried  
22 straps;  
  
23 top insulating material having a top insulator thickness extending up to a  
24 surface of said device layer in said trenches above said strap conductive  
25 material, whereby said top insulator thickness is approximately equal to  
26 said device layer thickness; and  
  
27 a set of isolating trenches extending through said device layer and said  
28 array insulating layer outside said trenches and said cell pass transistors, to

29 a depth of at least said bottom of said buried straps, said isolating trenches  
30 being filled with an isolating material, whereby only that portion of said  
31 buried strap inside said trenches and underneath said transistors remains  
32 and said buried straps are isolated from corresponding buried straps in  
33 adjacent cells by said isolating material, and whereby said pairs of cells  
34 having a trench capacitor in a first cell separated by a portion of material  
35 from a corresponding trench capacitor in an adjacent cell are separated by  
36 said isolating material, so that the space available for passing wordlines  
37 comprises top insulators in said pairs of cells and said isolating trench;  
  
38 a set of horizontal cell pass transistors in said device layer having cell  
39 electrodes, transistor gates disposed above said device layer and connected  
40 to a first subset of interconnect lines and internal electrodes in contact with  
41 said buried straps through said contact area and separated from an adjacent  
42 trench by said isolating trenches.

1 20. (New) An integrated circuit according to claim 19, further  
2 comprising strap conductive material disposed in said trenches to a level  
3 below said bottom surface of said device layer, whereby said strap  
4 conductive material makes contact with said device layer only on said  
5 bottom surface and said top insulating material has a top insulator  
6 thickness greater than said device layer thickness.

1     21. (New) An integrated circuit according to claim 19, further  
2     comprising:  
  
3     a first set of wordlines contacting transistor gates in said first subset of  
4     cells and extending as passing wordlines over trenches in said second  
5     subset of cells, said first set of wordlines passing over and being separated  
6     vertically from said buried straps in said second subset of cells by said top  
7     insulator thickness; and  
  
8     a second set of wordlines contacting transistor gates in said second subset  
9     of cells and extending as passing wordlines over trenches in said first  
10    subset of cells, said second set of wordlines being separated vertically  
11    from said buried straps in said first subset of cells by said top insulator  
12    thickness.